RAMAIAH
Institute of Technology

CURRICULUM

for the Academic year 2019 – 2020

ELECTRONICS AND COMMUNICATION ENGINEERING

V & VI SEMESTER B.E

RAMAIAH INSTITUTE OF TECHNOLOGY
(Autonomous Institute, Affiliated to VTU)
Bangalore – 560054.

About the Institute

Ramaiah Institute of Technology (RIT) (formerly known as M. S. Ramaiah Institute of Technology) is a self-financing institution established in Bangalore in the year 1962 by the industrialist and philanthropist, Late Dr. M S Ramaiah. The institute is accredited with "A" grade by NAAC in 2014 and all engineering departments offering bachelor degree programs have been accredited by NBA. RIT is one of the few institutes with prescribed faculty student ratio and achieves excellent academic results. The institute was a participant of the Technical Education Quality Improvement Program (TEQIP), an initiative of the Government of India. All the departments have competent faculty, with 100% of them being postgraduates or doctorates. Some of the distinguished features of RIT are: State of the art laboratories, individual computing facility to all faculty members. All research departments are active with sponsored projects and more than 150 scholars are pursuing PhD. The Centre for Advanced Training and Continuing Education (CATCE), and Entrepreneurship Development Cell (EDC) have been set up on campus. RIT has a strong Placement and Training department with a committed team, a good Mentoring/Proctorial system, a fully equipped Sports department, large air-conditioned library with over 1,35,427 books with subscription to more than 300 International and National Journals. The Digital Library subscribes to several online e-journals like IEEE, JET etc. RIT is a member of DELNET, and AICTE INDEST Consortium. RIT has a modern auditorium, several hi-tech conference halls and all are air-conditioned with video conferencing facilities. It has excellent hostel facilities for boys and girls. RIT Alumni have distinguished themselves by occupying high positions in India and abroad and are in touch with the institute through an active Alumni Association. RIT obtained Academic Autonomy for all its UG and PG programs in the year 2007. As per the National Institutional Ranking Framework, MHRD, Government of India, Ramaiah Institute of Technology has achieved 64th rank in 2019 among the top 100 engineering colleges across India.

About the Department

The Department of Electronics and Communication was started in 1975 and has grown over the years in terms of stature and infrastructure. The department has well equipped simulation and electronic laboratories and is recognized as a research center under VTU. The department currently offers a B. E. program with an intake of 120, and two M. Tech programs, one in Digital Electronics and Communication, and one in VLSI Design and Embedded Systems, with intakes of 30 and 18 respectively. The department has a Center of Excellence in Food Technologies sponsored by VGST, Government of Karnataka. The department is equipped with numerous UG and PG labs, along with R & D facilities. Past and current research sponsoring agencies include DST, VTU, VGST and AICTE with funding amount worth Rs. 1 crore. The department has modern research ambitions to develop innovative solutions and products and to pursue various research activities focused towards national development in various advanced fields such as Signal Processing, Embedded Systems, Cognitive Sensors and RF Technology, Software Development and Mobile Technology.

Vision of the Institute

To be an Institution of International Eminence, renowned for imparting quality technical education, cutting edge research and innovation to meet global socio-economic needs

Mission of the Institute

RIT shall meet the global socio-economic needs through

- *Imparting quality technical education by nurturing a conducive learning environment through continuous improvement and customization*
- *Establishing research clusters in emerging areas in collaboration with globally reputed organizations*
- *Establishing innovative skills development, techno-entrepreneurial activities and consultancy for socio-economic needs*

Quality Policy

We at Ramaiah Institute of Technology strive to deliver comprehensive, continually enhanced, global quality technical and management education through an established central Quality Management System complemented by the synergistic interaction of the stakeholders concerned.

Vision of the Department

To evolve into a department of national and international repute for excellence in education and cutting-edge research in the domain of Electronics and Communication Engineering

Mission of the Department

The department will continuously strive to

1. *Provide a world-class learning environment that caters to local and global technological and social requirements*
2. *Initiate research collaborations with academia and industries to perform cutting edge research leading to socio-technological innovations*
3. *Develop skills for pursuing innovation and entrepreneurial ventures for graduating engineers*

Program Educational Objectives (PEOs):

PEO1: *To train to be employed as successful professionals in a core area of their choice*

PEO2: *To participate in lifelong learning/ higher education efforts to emerge as expert researchers and technologists*

PEO3: *To develop skills in ethical, professional, and managerial domains*

Program Outcomes (POs):

PO1: *Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.*

PO2: *Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.*

PO3: *Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.*

PO4: *Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.*

PO5: *Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.*

PO6: *The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.*

PO7: *Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.*

PO8: *Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.*

PO9: ***Individual and team work:*** *Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.*

PO10: ***Communication:*** *Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.*

PO11: ***Project management and finance****: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.*

PO12: ***Life-long learning****: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.*

Program Specific Outcomes (PSOs):

PSO1: ***Circuit Design Concepts:*** *Apply basic and advanced electronics for implementing and evaluating various circuit configurations*

PSO2: ***VLSI and Embedded Domain:*** *Demonstrate technical competency in the design and analysis of components in VLSI and embedded domains*

PSO3: ***Communication Theory and Practice:*** *Possess application level knowledge in theoretical and practical aspects required for the realization of complex communication systems*

CURRICULUM COURSE CREDITS

DISTRIBUTION BATCH 2017-21

Semester	Humanities & Social Sciences (HSS)	Basic Sciences / Lab (BS)	Engineering Sciences/ Lab (ES)	Professional Courses - Core (Hard core, soft core, Lab) (PC-C)	Professional Courses - Electives (PC-E)	Other Electives (OE)	Project Work/Internship (PW/IN)	Extra & Co-curricular activities (EAC)	Total Credits in a Semester
First	02	09	14						**25**
Second	04	09	12						**25**
Third		08	07	10					**25**
Fourth		04		21					**25**
Fifth	02			19	04				**25**
Sixth				15	04		06		**25**
Seventh				14	12				**26**
Eighth						04	18	02	**24**
Total	**08**	**30**	**33**	**79**	**20**	**04**	**24**	**02**	**200**

SCHEME OF TEACHING

V SEMESTER

Sl. No.	Course Code	Course Title	Category	Credits					Contact Hours
				L	T	P	S	Total	
1.	EC51	Analog Communication	PC-C	4	0	0	0	4	4
2.	EC52	CMOS VLSI Design	PC-C	3	0	0	1	4	5
3.	EC53	Digital Signal Processing	PC-C	3	1	0	0	4	5
4.	EC54	Transmission Lines & Radiating Systems	PC-C	3	1	0	0	4	5
5.	EC55	Management, Entrepreneurship & IPR	PC-C	1	0	0	1	2	5
6.	ECExx	Departmental Elective	PC-E	3	0	0	1	4	7
7.	ECL56	Analog Communication & LIC Laboratory	PC-C	0	0	1	0	1	2
8.	ECL57	Digital Signal Processing Laboratory	PC-C	0	0	1	0	1	2
9.	ECL58	HDL & VLSI Laboratory	PC-C	0	0	1	0	1	2
			Total	17	2	3	3	25	37

VI SEMESTER

Sl. No.	Course Code	Course Title	Category	Credits					Contact Hours
				L	T	P	S	Total	
1.	EC61	Digital Communication	PC-C	3	1	0	0	4	5
2.	EC62	Microcontroller	PC-C	3	0	0	1	4	7
3.	EC63	Microwave Devices and Radar	PC-C	3	0	0	1	4	7
4.	EC64	Mini-Project (Optional: Interdisciplinary Projects)	PC-C	0	0	6	0	6	6
5.	ECExx	Departmental Elective	PC-E	3	0	0	1	4	7
6.	ECL65	Digital Communication Laboratory	PC-C	0	0	1	0	1	2
7.	ECL66	Microwaves & Antenna Laboratory	PC-C	0	0	1	0	1	2
8.	ECL67	Microcontroller Laboratory	PC-C	0	0	1	0	1	2
		Total		12	1	9	3	25	38

List of Electives

Sl. No.	Course Code	Course Title	Credits				
			L	T	P	S	Total
1.	ECE01	Power Electronics	3	0	0	1	4
2.	ECE02	Random Variables and Random Process	3	0	0	1	4
3.	ECE03	Speech Processing	3	0	0	1	4
4.	ECE04	Low Power VLSI design	3	0	0	1	4
5.	ECE05	Object Oriented Programming with C++	3	0	0	1	4
6.	ECE06	Digital System Design using Verilog	3	0	0	1	4
7.	ECE07	DSP Architecture & Algorithms	3	0	0	1	4
8.	ECE08	MEMS	3	0	0	1	4
9.	ECE09	Artificial Neural Networks & Fuzzy Logic	3	0	0	1	4
10.	ECE10	Image Processing	3	0	0	1	4
11.	ECE11	Real Time Systems	3	0	0	1	4
12.	ECE12	Advanced Digital Logic Design	3	0	0	1	4
13.	ECE13	Advanced Digital Logic Verification	3	0	0	1	4
14.	ECE14	Linear Algebra	3	0	0	1	4
15.	ECE15	Machine Learning	3	0	0	1	4
16.	ECE16	Analog and Mixed Signal VLSI Design	3	0	0	1	4
17.	ECE17	Neural Networks and Deep Learning	3	0	0	1	4
18.	ECE18	Advanced Embedded Systems	3	0	0	1	4
19.	ECE19	Multi-resolution Signal Processing	3	0	0	1	4
20.	ECE20	Modeling and Simulation of Data Networks	3	0	0	1	4
21.	ECE21	Cyber Security	3	0	0	1	4
22.	ECE22	Distributed Systems	3	0	0	1	4
23.	ECE23	Optical Networks	3	0	0	1	4
24.	ECE24	Internet Engineering	3	0	0	1	4
25.	ECE25	Multimedia Communication	3	0	0	1	4
26.	ECE26	RTOS	3	0	0	1	4
27.	ECE27	GSM Network	3	0	0	1	4
28.	ECE28	Ad-hoc Wireless Networks	3	0	0	1	4
29.	ECE29	Cryptography and Network Security	3	0	0	1	4
30.	ECE30	Advanced Computer Architecture	3	0	0	1	4

ANALOG COMMUNICATION

Course Code: EC51   **Credits: 4:0:0:0**
Prerequisites: Signals and Systems   **Contact Hours: 56**
Course Coordinator: Lakshmi S

UNIT – I

Amplitude Modulation and Double Side-band Suppressed Carrier Modulation: Introduction to AM: Time domain description, Frequency domain description. Generation of AM wave: Square law modulator, switching modulator. Detection of AM waves: Square law detector, envelope detector, time domain description of DSBSC, Frequency domain representation, Generation of DSBSC waves, balanced modulator, ring modulator, coherent detection of DSBSC modulated waves, Costas loop, Quadrature carrier multiplexing.

UNIT – II

Single Side-band Modulation (SSB): Hilbert transform, properties of Hilbert transform, pre-envelope, single side-band modulation, frequency domain description of SSB wave, time domain description of SSB wave, frequency discrimination method for generating an SSB modulated wave, phase discrimination method for generating an SSB modulated wave, demodulation of SSB waves.

Vestigial Side-band Modulation: Frequency domain description, Generation of VSB modulated wave, time domain description, coherent demodulation, envelope detection of VSB wave along with carrier.

UNIT – III

Angle Modulation (FM): Basic definitions, FM, narrow band FM, wideband FM, transmission bandwidth of FM waves. Generation of FM waves: indirect FM and direct FM, frequency stabilization in FM receivers, Demodulation of FM waves: frequency discrimination method, phase locked loop, nonlinear model of phase locked loop, linear model of the phase locked loop, nonlinear effect in FM systems.

UNIT – IV

Applications of AM and FM: AM radio (super heterodyne): Block diagram of transmitter and receiver, mixer, AGC, performance characteristics. FM radio: block diagram of transmitter and receiver.

Elements of Color TV: Frequency range and channel bandwidth, scanning and synchronization, composite video signal. Block diagram of transmitter and receiver.

UNIT – V

Noise Basics and Noise in Continuous Wave Modulation Systems: Introduction, shot noise, thermal noise, white noise, noise equivalent bandwidth, noise figure, equivalent noise temperature, cascade connection of two port networks, receiver model, noise in DSBSC receivers, noise in SSB receivers, noise in AM receivers, threshold effect, noise in FM receivers, FM threshold effect, pre-emphasis and de-emphasis in FM.

Textbooks:

1. Simon Haykin, and Michael Moher, "Communication Systems", 5th Edition, John Wiley, 2009.
2. George Kennedy, Bernard Davis, S R M Prasanna, "Electronic Communication Systems", 5th Edition, McGraw Hill, 2011.

References:

1. Simon Haykin, "An Introduction to Analog and Digital Communication", 2nd Edition, Wiley India Pvt Ltd., 2012.
2. H. Taub, D. L. Schilling, "Principles of Communication Systems", 2nd Edition, McGraw Hill, Reprint, 2008.
3. R. R. Gulati, "Monochrome and Colour TV", 3rd Edition, New Age International (P) Ltd. 2014.

Course Outcomes (COs):

1. Analyze the generation and demodulation of AM and DSBSC systems. (POs – 1, 2, 3, 4, 12, PSOs – 1, 3)
2. Realize the generation and demodulation of SSB and VSB. (POs – 1, 2, 3, 4, 12, PSOs – 1, 3)
3. Discuss the direct and indirect method of generation of FM and its detection. (POs – 1, 2, 3, 4, 12, PSOs – 1, 3)
4. Apply AM and FM basics in radio and TV systems. (POs – 2, 3, 12, PSOs – 1, 3)
5. Analyze the noise performance of receivers. (POs – 1, 2, 12, PSOs – 1, 3)

CMOS VLSI DESIGN

Course Code: EC52   **Credits: 3:0:0:1**
Prerequisites: Digital Electronic Circuits   **Contact Hours: 42**
Course Coordinator: A. R. Priyarenjini

UNIT – I

CMOS Logic and Layouts: Introduction and history, CMOS Logic Circuits: Logic Gates, Pass Transistor and Transmission gates.

CMOS Fabrication and Layouts: Inverter Cross Section, Fabrication Process, Layout Design Rules, Gate Layout, Stick Diagrams, Fabrication, Packaging and Testing.

UNIT – II

MOS Transistor Theory: Ideal V-I Characteristics, C-V Characteristics: simple MOS capacitance models, Detailed MOS Gate Capacitance model, Detailed MOS diffusion capacitance model, Non-ideal V-I Effects, DC Transfer Characteristics, Switch level RC delay model.

UNIT – III

Circuit Characterization and Performance Estimation: Delay Estimation: RC delay model, linear delay model, Logical Effort (LE), LE and Transistor Sizing: Delay in gates and multistage networks, choosing the best number of stages with LE, Power Dissipation.

UNIT – IV

Combinational Circuit Design: Circuit Families: Static CMOS, Ratioed Circuits, CVSL, Dynamic Circuits, Pass Transistor Circuits.

UNIT – V

Data path Subsystems: Adders: Ripple carry, Carry Generate and Propagate, Propagate Generate Logic, Manchester Carry Chain, Carry Skip, Carry Select, Carry Look ahead, Tree Adders, Subtraction, Multiple-Input Addition.

Self Study: VLSI Design Flow, Design specification, Design entry, Functional Simulation, Placement and Routing, Timing Simulation, Fabrication into the chip, CMOS Technologies, Design Margins, Reliability, Comparison of circuit families, Historical Perspectives, One/Zero Detectors.

Textbooks:

1. Neil Weste and David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, Tata McGraw Hill, 2010.
2. Sung Mo Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits", 4th Edition, McGraw Hill, 2014.

References:

1. Jan Rabaey, B. Nikolic, A. Chandrakasan, "Digital Integrated Circuits: A Design Perspective", 2nd Edition, Pearson, 2003.
2. Morris Mano and Michael Ciletti, "Digital Design", 4th Edition, Prentice Hall, 2006.

Course Outcomes (COs):

1. Create MOS schematics and corresponding layouts for simple digital logic functions. (POs– 2, 3, 4, 5, 9, 10, 11, PSO – 2)

2. Calculate various circuit parameters such as current and device capacitance for a MOS transistor. (POs – 2, 3, 4, 5, 9, 10, 11, PSO – 2)

3. Evaluate the delay due to a MOS logic circuit, and thereby design a circuit to satisfy certain design parameters. (POs – 2, 3, 4, 5, 9, 10, 11, PSO – 2)

4. Analyze the performance of various MOS circuit families. (POs – 2, 3, 4, 5, 9, 10, 11, PSO – 2)

5. Describe various connection configurations to realize digital adder designs and analyze their operating speed. (POs – 2, 3, 4, 5, 9, 10, 11, PSO – 2)

DIGITAL SIGNAL PROCESSING

Course Code: EC53   **Credits: 3:1:0:0**
Prerequisite: Signals and Systems   **Contact Sessions: 56**
Course Coordinator: K. Indira

UNIT – I

Sampling and Reconstruction of Signals: Ideal sampling and reconstruction of continuous time signals, discrete time processing of continuous time signals.

Frequency Domain analysis of LTI systems: Frequency domain characteristics of LTI systems, Frequency response of LTI systems, Frequency Domain Sampling and Reconstruction of discrete time signals.

UNIT – II

DFT and FFT: Discrete Fourier Transform, DFT as a linear transformation, Properties of DFT, DFT in linear filtering, Filtering long data sequences: overlap-save method, overlap-add method, FFT algorithms: Direct computation of DFT, Radix-2 FFT algorithm: Decimation-in-time algorithm, Decimation-in-frequency algorithm.

UNIT – III

FIR Filters: Design of FIR filters: Symmetric and anti-symmetric FIR filters, Design of linear-phase FIR filters using windows and frequency sampling methods, FIR differentiators.

Structures for FIR Systems: Direct-Form Structures, Cascade-Form Structures and Lattice Structures.

UNIT – IV

IIR Filters: Analog filter specifications, Classification of Analog filters: Butterworth and Chebyshev filters, Frequency transformations, Design of Analog filters, Digital IIR filter design using impulse invariant method, bilinear transformation, Matched z-transform methods.

IIR filter structures: Direct form (I and II), Cascade, Parallel, and Transposed structures

UNIT – V

Architecture and Instruction set of TMS320C67x Processor: Architecture, Addressing modes, Instruction sets, Assembler directives, Memory considerations, Fixed and Floating point formats, implementation of FIR and IIR filters.

Textbooks:

1. J. G. Proakis and D. G. Manolakis, "Digital Signal Processing: Principles, Algorithms and Applications", 4th Edition, Pearson Education Asia/Prentice Hall of India, 2014.
2. Rulph Chassaing, Donald Relay, "Digital Signal Processing and Applications with TMS3206713 and TMS320C6416DSK", 2nd Edition, Wiley Publications, 2014.

References:

1. Alan V. Oppenheim, Ronald W. Schafer, "Discrete Time Signal Processing", 3rd Edition, Pearson Education, 2014.
2. Sen M. Kuo, Woon-Seng S. Gan, "Digital Signal Processors: Architectures, Implementations and Applications", Pearson/Prentice Hall, 2005.
3. Emmanuel Ifeachor, Barrie W. Jervis, "Digital Signal Processing: A Practical Approach", 2nd Edition, Pearson Education, 2002.

Course Outcomes (COs):

1. Illustrate the importance of sampling and frequency domain analysis of LTI Systems. (POs – 1, 2, PSO – 3)

2. Apply DFT in linear filtering. (POs – 2, 3, PSO – 3)

3. Design and develop digital structures for FIR filters. (POs–2, 3, PSO – 3)

4. Design and develop digital structures for IIR filters. (POs – 2, 3, PSO – 3)

5. Summarize the architecture and instruction sets of TMS32067x processor. (POs– 2, 3, PSO –3)

TRANSMISSION LINES AND RADIATING SYSTEMS

Course Code: EC54   **Credits: 3:1:0:0**
Prerequisite: Electromagnetics   **Contact Sessions: 56**
Course Coordinator: Sujatha B

UNIT – I

Transmission Line theory: Lumped element circuit model for a transmission line, wave propagation on a transmission line and general solutions of line, terminated lossless line, characteristic impedance, reflection coefficient, VSWR and impedance equation. Special cases of terminated lossless line, Smith chart: construction and applications, Conventional and graphical solution of line parameters.

UNIT – II

Impedance matching and tuning, Line resonators: Matching with lumped elements (L-networks) only Smith chart solutions, Single stub tuning: Shunt and Series stubs, Quarter Wave transformer: Bandwidth performance of the transformer, Series and parallel resonant circuits: loaded Q and unloaded Q, Transmission line resonators.

UNIT – III

Transmission lines and Fundamentals of radiator: Co-axial line, Strip line and Micro strip line, Principle of antenna, fields from oscillating dipole, antenna field zones, basic antenna parameters, patterns, beam area, Radiation intensity, beam efficiency, directivity and gain, antenna aperture, effective height and radio communication link (Friis formula).

UNIT – IV

Point source and Arrays: Point source, Types of Arrays (Broad side, End fire, Extended End fire), Arrays of two point sources, linear array of n-isotropic point sources of equal amplitude and spacing, null direction for arrays with n isotropic point source of equal amplitude and spacing, pattern multiplication.

UNIT – V

Thin linear antenna, Horn antenna and Parabolic reflectors: Introduction, short electric dipole, Fields of short electric dipole, radiation resistance of short electric dipole, thin linear antenna, field components of $\lambda/2$ (hertz) dipole antenna, radiation resistance of $\lambda/2$ antenna, Directivity of dipole antenna, Types of antenna – Yagi-Uda antenna, Horn antenna, parabolic reflectors.

Textbooks:

1. David M. Pozar, "Microwave Engineering", 3rd Edition, Wiley, 2011.
2. John D Kraus, Ronald J Marhetka, Ahmad S Khan, "Antennas and Wave Propagation", 4th Edition, Tata McGraw Hill, 2010.

References:

1. John Ryder D, "Networks, Lines and Fields", Pearson India, 2015.
2. Constantine A Balanis, "Antenna, Theory, Analysis & Design", 4th Edition, John Wiley & Sons, 2016.

Course Outcomes (COs):

1. Analyze various transmission lines and find their parameters analytically and graphically. (POs – 1, 2, 3, 12, PSOs – 1, 2).

2. Apply Smith chart to design various impedance matching networks and also analyze line resonators. (POs – 1, 2, 3, 12, PSOs –1, 2).

3. Define the parameters of antenna. (POs – 1, 2, 3, 12, PSOs – 1, 3).

4. Design different types of arrays and study the concept of pattern multiplication. (POs – 1, 2, 3, 12, PSOs – 1, 3).

5. Explore the field components and radiation resistance of various antennas. (POs – 1, 2, 3, 12, PSOs – 1, 3).

MANAGEMENT, ENTREPRENEURSHIP AND IPR

Course Code: EC55   **Credits: 1:0:0:1**
Prerequisite: Nil   **Contact Hours: 14**
Course Coordinator: V. Nuthan Prasad

UNIT – I

Management: Introduction, functions of management, Roles of manager, Levels of management, Development of management thought.

Planning: Planning process, Types of plans (meaning only), Steps in planning, Decision making.

Organizing and Staffing: Principles of organization, Types of organization, Importance of staffing.

UNIT – II

Directing and Controlling: Principles of directing, Leadership styles, Techniques and importance of coordination and steps in controlling.

Entrepreneur: Functions of an entrepreneur, Stages in entrepreneurial process.

UNIT – III

SSI: Role of SSI in Economic Development, Steps to start an SSI.

Project Management: Project Identification, Project selection.

Entrepreneurship Development and Government: KIADB, MSME, SIDBI.

UNIT – IV

IPR: Basic Principles of IPR laws, history of IPR–GATT, WTO, WIPO and TRIPS, role of IPR in R&D and Knowledge era, concept of property, justification, Marx's theory of property, different forms of IPR.

UNIT – V

Patent: Evolution of patent law in India, Justifications, subject matters of patent, Criteria for patentability, patentable and non-patentable inventions, pre-grant and post-grant oppositions, grant or refusal of patents.

Patent application procedure and drafting: Patent drafting, format, provisional and complete specifications, scopes of invention, claims, patent search and types of patent searches.

Self Study: Modern management approaches, planning premises, Departmentation, committees, communication meaning and importance, methods of establishing control (in brief). Types of Entrepreneur, role of Entrepreneur in Indian economy and developing economies with reference to Self-employment development, impact of liberalization, privatization, globalization on SSI, project report, KSFC, constitutional aspects of intellectual property, infringement of patents and design rights.

Textbooks:

1. P. C. Tripathi, P. N. Reddy, "Principles of Management", 5th Edition, McGraw Hill, 2016.
2. Vasant Desai, "Dynamics of Entrepreneurial Development & Management", 4th Edition, Himalaya Publishing House, 2010.
3. P. Ganguli, "Intellectual Property Rights", Tata McGraw Hill, 2007.
4. T. Ramakrishna, "Course Material for I Year P. G. Diploma in IPR", NLSIU, Bangalore.

References:

1. Robert Lussier, "Management Fundamentals – Concepts, Application, Skill Development", 5th Edition, Thomson, 2012.
2. World Intellectual Property Organization Handbook/Notes, 2nd Edition, WIPO Publication, 2008.

Course Outcomes (COs):

1. Identify the importance of managerial discipline. (POs – 1, 2, 4, 5, 6, 7, 8, 9, 10, 11, 12, PSO – 2)
2. Interpret the concepts of directing and controlling. (POs – 1, 2, 5, 7, 8, 9, 10, 11, 12, PSO – 2)
3. Demonstrate the functions of an entrepreneurship development and describe various institutional supports (POs – 1, 4, 5, 6, 7, 8, 9, 10, 11, 12, PSO – 3)
4. Describe the basic principles of different IPRs (POs – 2, 7, 9, 10, 11, 12, PSO – 3)
5. Recognize the characteristics and infringement of patents (POs – 5, 6, 8, 9, 10, 11, 12, PSO – 3)

ANALOG COMMUNICATION AND LIC LABORATORY

Course Code: ECL56   **Credits: 0:0:1:0**
Prerequisites: Analog Electronic Circuits Laboratory   **Contact Sessions: 14**
Course Coordinator: Lakshmi S

LIST OF EXPERIMENTS

1. Differentiator and integrator using op-amps
2. Second order active low pass and high pass filter
3. Precision rectifier & 723 Regulator
4. Class-C amplifier
5. Generation and demodulation of AM
6. Schmitt Trigger
7. Generation of DSBSC using ring modulation
8. 555 Timer: Astable and Mono stable Multi vibrators
9. Generation and demodulation of FM
10. R-2R Ladder type Analog to Digital Converter and Flash ADC
11. Up conversion and down conversion using transistor mixer
12. Simulation of analog modulation techniques

Textbooks:

1. Simon Haykin and Michael Moher, "Communication Systems", 5th Edition, John Wiley, 2009.
2. George Kennedy, Bernard Davis, S R M Prasanna, "Electronic Communication Systems", 5th Edition, McGraw-Hill, 2011.
3. David A. Bell, "Operational Amplifiers and Linear IC's", PHI/Pearson, 3rd Edition, 2011.
4. D. Roy Choudhury and Shail B. Jain, "Linear Integrated Circuits", 2nd Edition, New Age International Reprint, 2006.

Course Outcomes (COs):

1. Analyze basic op-amp circuits to perform differentiation and integration. (POs – 1, 2, 3, 4, 9, 10, PSOs – 1, 3)
2. Design, simulate and implement modulation and demodulation circuits for AM and FM (POs – 1, 2, 3, 4, 5, 9, 10, PSOs – 1, 3)
3. Test analog filters, precision rectifier and regulators for the given specifications (POs – 1, 2, 3, 4, 9, 10, PSOs – 1, 3)
4. Implement multi vibrators using IC555 timer for the given specifications (POs – 1, 2, 3, 4, 9, 10, PSOs – 1, 3)
5. Construct analog to digital converters. (POs – 1, 2, 3, 4, 9, 10. PSOs –1, 3)

DIGITAL SIGNAL PROCESSING LABORATORY

Course Code: ECL57   **Credits: 0:0:1:0**
Prerequisite: Signals and Systems   **Contact Sessions: 14**
Course Coordinator: K. Indira

LIST OF EXPERIMENTS

Simulation Experiments

1. Verification of Sampling Theorem
2. DFT and IDFT, Circular convolution and Linear convolution
3. Design and implementation of FIR Filters (LP, HP, BP, BS) by using window techniques
4. Design and implementation of analog IIR Filters (Butterworth and Chebyshev)
5. Design and implementation of digital IIR Filters (Bilinear transformation)

Hardware Experiments

6. Linear convolution and Circular convolution
7. Computation of N point DFT/IDFT
8. Response of a discrete time system
9. Design and implementation of digital FIR Filters
10. Design and implementation of digital IIR Filters
11. Filtering of noisy signal using FIR filter
12. Generating signals of different frequencies and construction of AM wave

Textbooks:

1. J. G. Proakis and Ingle, "Digital signal processing using MATLAB", 3rd Edition, Cengage Learning, 2014.
2. Sanjit K. Mitra, "Digital Signal Processing", 4th Edition, Tata McGraw Hill, 2014.

Course Outcomes (COs):

1. Apply sampling theorem on continuous time signal. (POs – 1, 2, 3, 5, 9, PSO – 3)
2. Apply DFT and IDFT in linear and circular convolutions. (POs –1, 2, 3, 5, 9, PSO – 3)
3. Analyze the frequency response of FIR and IIR filters. (POs – 2, 3, 5, 9, PSO – 3)
4. Demonstrate filtering of noisy signals. (POs – 2, 3, 4, 5, 9, PSO – 3)
5. Discuss generation of AM wave. (POs – 2, 3, 4, 5, 9, PSO – 3)

HDL AND VLSI LABORATORY

Course Code: ECL58   **Credits: 0:0:1:0**
Prerequisite: Digital Design   **Contact Sessions: 14**
Course Coordinator: A. R. Priyarenjini

LIST OF EXPERIMENTS

All the experiments will make use of appropriate design tools.

1. Introduction to Design Entry and Simulation
2. Net list generation, power, area, and timing report generation
3. NMOS and PMOS DC Analysis
4. Device Characterization
5. CMOS Inverter DC and Transient analysis
6. Propagation delay of various simple gates, and comparison with logical effort
7. Fanout-of-4 Inverter delay measurement in different technologies
8. Verification of method of Logical effort
9. Inverter Chain Sizing
10. Verification of Full adder implementations at the transistor level
11. Inverter Layout Design and Post layout simulation

Textbook:

1. Neil Weste and David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, Tata McGraw Hill, 2010

Course Outcomes (COs):

1. Employ the digital design tools for HDL design entry, simulation, and synthesis. (POs– 2, 3, 4, 5, 9, 10, PSO – 2)
2. Create and verify functionality of various gates at the transistor level. (POs– 2, 3, 4, 5, 9, 10, PSO – 2)
3. Measure circuit performance parameters by performing simulations of circuit configurations. (POs– 2, 3, 4, 5, 9, 10, PSO – 2)
4. Use tools to characterize processes by conducting suitable experiments. (POs– 2, 3, 4, 5, 9, 10, PSO – 2)
5. Create the layout for simple gates, and perform RC extraction and post layout simulation. (POs– 2, 3, 4, 5, 9, 10, PSOs – 2)

DIGITAL COMMUNICATION

Course Code: EC61   **Credits: 3:1:0:0**
Prerequisites: Analog Communication   **Contact Sessions: 56**
Course Coordinator: Sadashiva V Chakrasali

UNIT – I

Signal Sampling: Basic signal processing operations in digital communication, Sampling Principles, Sampling Theorem, Quadrature sampling of band-pass signals, Practical aspects of sampling and signal recovery, PAM, TDM.

UNIT – II

Waveform Coding Techniques: PCM block diagram, Different quantization techniques, SNR in PCM, Robust quantization, DPCM, DM, Adaptive DM.

Base-Band Shaping for Data Transmission: Line Codes and their power spectra.

UNIT – III

Inter symbol interference: Introduction, Nyquist criterion for distortion less base-band binary transmission, correlative coding, duo binary coding, Eye pattern.

Detection: Model of digital communication system, Gram–Schmidt orthogonalization, geometric interpretation of signals, Maximum likelihood estimation.

UNIT – IV

Detection: Correlation receiver, Matched Filter Receiver, Properties of Matched Filter.

Digital Modulation and Demodulation Techniques: Coherent binary modulation techniques, BPSK, FSK, ASK, QPSK systems with signal space diagram, generation, demodulation and error probability concept, Comparison using Power Spectrum.

UNIT – V

Non coherent modulation techniques: FSK and BPSK, DPSK.

Spread spectrum modulation: Pseudo noise sequences, Notion of spread spectrum, direct sequence spread coherent BPSK, Signal space dimensionality and processing gain, Frequency Hop spread spectrum and applications of spread spectrum modulation.

Textbooks:

1. Simon Haykin, "Digital Communications", John Wiley, Reprint 2014.
2. B. P. Lathi and Zhi Ding, "Modern Digital and Analog Communication Systems", International 4th Edition, Oxford University Press, 2015.

References:

1. Simon Haykin, "An Introduction to Analog and Digital Communication", John Wiley, 2003.
2. Bernard Sklar "Digital Communications", Pearson Education, 2007.

Course Outcomes (COs):

1. Design a system to convert the given analog signal into discrete signal. (POs – 1, 2, 3, 8, 11, PSO – 3)
2. Analyze PCM, DPCM, DM and ADM systems and Base Band shaping for data transmission. (POs – 1, 2, 3, 4, 8, 11, PSO – 3)
3. Describe effects of ISI and detect message signal in noisy environment. (POs – 1, 2, 3, 4, 8, 11, PSO – 3)
4. Compare performance of BPSK, ASK, and QPSK systems and their power spectra. (POs – 1, 2, 3, 8, 11, PSO – 3)
5. Describe spread spectrum technology and its applications. (POs – 1, 2, 3, 8, 11, PSO – 3)

MICROCONTROLLER

Course Code: EC62   **Credits: 3:0:0:1**
Prerequisite: Microprocessors   **Contact Hours: 42**
Course Coordinator: Sara Mohan George

UNIT – I

The MSP430 Architecture: The outside view-pin out, the inside view, memory, CPU, Memory mapped input output Addressing Modes, Constant generator and emulated instructions, Instruction set, examples

UNIT – II

Functions and subroutines: Storage for local variables, passing parameters to a subroutine and returning a result, mixing C and assembly language, interrupts, interrupt service routines, interrupt service routines in C, non-maskable interrupts, issues associated with interrupts, Low power modes

Digital input, output and displays: Parallel ports, digital inputs, interrupts on digital inputs, multiplexed inputs: scanning a matrix keypad, Digital outputs: multiplexed displays.

UNIT – III

Timers: Watchdog timer, timer A: Timer block, capture/compare channels, interrupts from timer A, Measurement in the capture mode: Measurement of time; Press and release of button, Output in the continuous mode: Generation of Independent, Periodic Signals, Output in the Up Mode: Edge-Aligned PWM, simple PWM, design of PWM.

UNIT – IV

Mixed signal systems: Comparator_A+, Architecture of Comparator_A+, Operation of Comparator_A+, Analog to digital conversion: general issues, Resolution, Precision, and Accuracy, SD 16 sigma delta ADC, signal conditioning and operational amplifiers: Thermistor for range 5°C – 30°C.

UNIT – V

Communication: Communication peripherals in MSP430, serial peripheral interface, SPI with USI, Inter-integrated circuit bus: Hardware for I2C, I2C protocol.

Self Study: Clock generator, driving an LCD from an MSP430x4xx, Basic timer1, real time clock, Architecture of Sigma Delta ADC, Asynchronous serial communication.

Textbook:

1. John H Davies, "MSP430 Microcontrollers Basics", 1st Edition, Newnes Publishers, 2008.

Reference:

1. C. P. Ravikumar, "MSP430 Microcontroller in Embedded System Projects", Elite Publishing House, New Delhi, 2012.

Course Outcomes (COs):

1. Explain the addressing modes, generation of constants and instruction sets of MSP430 microcontroller. (POs – 1, 3, PSOs –1, 2)
2. Demonstrate the interfacing of various devices to the input and output pins of MSP430 using Interrupt Service Routines. (POs – 1, 4, PSOs –1, 2)
3. Generate independent periodic and PWM signals using different modes of MSP430 timer. (POs – 1, 3, PSOs – 1, 2)
4. Design the conversion of analog inputs to digital outputs using comparator A+ and Sigma Delta ADC. (POs – 1, 4, PSOs – 1, 2)
5. Describe communication between peripherals using SPI and I2C. (POs – 1, 3, PSOs – 1, 3)

MICROWAVE DEVICES AND RADAR

Course Code: EC63   **Credits: 3:0:0:1**

Prerequisites: Transmission Lines & Radiating Systems   **Contact Hours: 42**

Course Coordinator: Sujatha B

UNIT – I

Multiport Microwave Network Analysis: Scattering matrix–reciprocal networks and lossless networks, shift in reference planes, Basic properties of dividers and couplers – three-port networks, four-port networks; T-junction power divider – lossless divider, resistive divider, Wilkinson power divider – even-odd mode analysis.

UNIT – II

Microwave Passive and Active devices: Composite filter design by the image parameter method, PIN diodes, Phase shifters, Schottky-barrier diode, Attenuator, RWH theory, Gunn diodes– Gunn effect, modes of operation.

UNIT – III

Microwave Tubes: Introduction, Klystrons: Two cavity klystron amplifiers, Multicavity Klystron Amplifiers, Reflex Klystrons: Mathematical analysis of power and efficiency, Traveling Wave Tubes, Magnetron Oscillators.

UNIT – IV

Introduction to Radar: Basic Radar–Principle of operation, Simple form of the Radar Equation, Radar Block Diagram, Radar Frequencies, Applications of Radar.

Radar Equation: Introduction, Detection of signals in noise, Receiver noise and signal-to-noise ratio, Radar cross-section of Targets.

UNIT – V

Special types of Radar: CW Radar, Coherent MTI Radar–Delay line cancellers, Blind speeds, Digital MTI processor, Pulse Doppler Radar, Tracking Radar, Synthetic Aperture Radar (SAR), Air Surveillance Radar, Electronic Counter Measure, Bistatic Radar.

Self Study: Impedance, admittance and transmission matrices of reciprocal microwave networks and lossless microwave networks, Stepped-impedance low-pass filters, varactor diode and its applications, IMPATT diode and its applications, conventional vacuum tubes comparison, applications of Klystron amplifier, oscillator, applications of TWTA, applications of magnetron oscillator, origins of radar, applications of radar, Doppler effect, millimeter waves radar**.**

Textbooks:

1. David M. Pozar, "Microwave Engineering", 3rd Edition, Wiley, 2011.
2. Samuel Y Liao, "Microwave Devices and Circuits", 3rd Edition, Pearson, 2011.
3. Merrill I. Skolnik, "Introduction to Radar Systems", 3rd Edition, Tata McGraw Hill, 2015.

References:

1. Annapurna Das and Sisir K Das, "Microwave Engineering", 2nd Edition, McGraw-Hill 2009.
2. Robert E. Collin "Foundations of Microwave Engineering", 2nd Edition, Wiley, 2005.

Course Outcomes (COs):

1. Apply the properties of scattering parameters to obtain the S-matrix of microwave components and circuits. (POs – 1, 2, PSO – 3)
2. Examine the consequence of various microwave passive & active devices and design the Microwave filters. (POs – 1, 2, 3, 10, PSO – 3)
3. Illustrate the significance of various microwave tubes. (POs – 1, 2, 10, PSO – 3)
4. Interpret the importance of radar and radar range equation. (POs – 1, 2, 10, PSO – 3)
5. Outline the key role played by special types of radar. (POs – 1, 10, PSO – 3)

MINI PROJECT

Course Code: EC64   **Credits: 0:0:6:0**

Students will commence and complete a technical project under the guidance of a faculty member in the department. The quality of the work will be judged in two presentations, where the panel consists of the guide and at least two other faculty members in the project domain.

Subject Code	Subject	No. of Hrs/Week		Duration of Exam (Hrs)	Marks		Total Marks	Credits
		Lecture	Practical/ Field Work		IA	Exam		
EC64	Mini-project	-	-	-	50	-	50	6

Course Outcomes (COs):

1. Perform a survey of existing methods in the domain of the chosen topic. (POs – 1, 2, 3, 4, PSO-1)
2. Describe the proposed design in terms of its technical block diagram. (POs – 2, 3, 10, PSOs – 2, 3)
3. Implement the technical block diagram using appropriate tools. (POs – 2, 3, 4, 5, PSOs – 2, 3)
4. Conduct extensive experimentation to evaluate the quality of the design. (POs – 2, 3, 4, 5, PSOs – 2, 3)
5. Present and prepare technical details of the project at regular intervals. (POs – 9, 10, PSOs – 2, 3)

DIGITAL COMMUNICATION LABORATORY

Course Code: ECL65   **Credits: 0:0:1:0**
Prerequisites: Analog Communication   **Contact Sessions: 14**
Course Coordinator: Sadashiva V Chakrasali

LIST OF EXPERIMENTS

1. Verification of sampling theorem
2. Time Division Multiplexing
3. Generation and detection of Amplitude Shift Keying signals
4. Generation and detection of Frequency Shift Keying signals
5. Generation and detection of Phase Shift Keying signals
6. Generation and detection of Quadrature PSK & DPSK
7. PCM modulation and demodulation
8. Delta modulation and demodulation
9. Simulation for verification of sampling theorem
10. Simulation for performance analysis of various digital modulation and demodulation techniques

Textbooks:

1. Simon Haykin, "Digital Communications", John Wiley, Reprint 2014.
2. J. G. Proakis and M. Salehi, "Contemporary Communication Systems using MATLAB", PWS Publishing Company, 2007.

Course Outcomes (COs):

1. Implement a sampling circuit to find Nyquist rate. (POs – 1, 2, 3, 5, 6, 8, 11, PSO – 3)
2. Employ TDM for band limited signals. (POs – 1, 2, 11, PSO – 3)
3. Design and implement ASK, PSK, FSK, DPSK digital modulation schemes. (POs – 3, 4, 7, 11, PSO – 3)
4. Design and implement PCM and Delta modulation scheme. (POs – 3, 4, 5, 7, 11, PSO – 3)
5. Analyze the performance of various modulation techniques. (POs – 2, 4, 11, PSO – 3)

MICROWAVE AND ANTENNAS LABORATORY

Course Code: ECL66   **Credits: 0:0:1:0**
Prerequisite: Transmission Line & Radiating Systems   **Contact Sessions: 14**
Course Coordinator: Sujatha B

LIST OF EXPERIMENTS

1. Verify the power division and calculate insertion loss and isolation of a hybrid network (Magic tee).
2. Determination of coupling and isolation characteristics of a micro strip, branch line directional coupler
3. Determination of coupling and isolation characteristics of a micro strip backward directional coupler
4. Measurement of resonance characteristics of a micro strip ring resonator and determination of dielectric constant
5. Measurement of power division and isolation characteristics of a micro strip 3 dB power divider
6. Verify the power division and calculate insertion loss and isolation of a waveguide directional coupler
7. Characteristics of Gunn diode
8. Mode curves of Reflex Klystron
9. Radiation pattern and directivity of Horn antenna
10. Radiation pattern and directivity of Yagi-uda antenna
11. Radiation pattern and directivity of dipole antenna
12. Radiation pattern and directivity of patch antenna

Textbooks:

1. David M. Pozar, "Microwave Engineering", 3rd Edition, Wiley, 2011.
2. Samuel Y Liao, "Microwave Devices and Circuits", 3rd Edition, Pearson, 2011.
3. John D. Kraus , Ronald J. Marhefka and Ahmad S Khan "Antennas and Wave Propagation", 4th Edition, McGraw-Hill Publications, 2006.

Course Outcomes (COs):

1. Analyze the characteristics of multiport waveguide microwave networks. (POs – 1, 2, 9, 10, PSO – 3)
2. Interpret the characteristics of microwave oscillators. (POs –1, 2, 9, 10, PSO – 3)
3. Obtain the radiation pattern and calculate the directivity and gain of horn antenna. (POs – 1, 2, 9, 10, PSO – 3)
4. Calculate the parameters of printed antennas (POs – 1, 2, 9, 10, PSO – 3)
5. Analyze the power division in micro-strip microwave network. (POs – 1, 2, 9, 10, PSO – 3)

MICROCONTROLLER LABORATORY

Course Code: ECL67   **Credits: 0:0:1:0**

Prerequisite: Microprocessors   **Contact Sessions: 14**

Course Coordinator: Sara Mohan George

LIST OF EXPERIMENTS

Part A: Assembly Language Programming

1. Data block move : with overlap, without overlap and interchange

2. Addition, subtraction, multiplication and division of N-bit multi precision numbers (N > 32 bits)

3. Identify whether a given number is positive, negative, odd and even

4. Sorting and finding smallest/largest element in an array

5. Code conversion between BCD, ASCII & Hexadecimal

6. Square, cube, LCM, HCF and factorial of a number

7. Addition and subtraction of two string ASCII digits

8. String transfer and string reversal

9. Identify whether a string is palindrome

Part B: Interfacing

Write C programs to interface MSP430 with peripherals:

10. Toggle LEDs using Timer A to set delay
11. Identify a key press by interfacing keypad with 7 segment display
12. Display on LCD: a key pressed or a message on the LCD module

13. Seven segment interface: 4 digit up/down binary and decimal counter
14. Generating pulse width modulation

Textbook:

1. John Davies, "MSP430 Microcontroller Basics**",** Elsevier, 2008.

Reference:

1. C. P. Ravi kumar, "MSP430 Microcontroller in Embedded System Projects", Elite Publishing House, New Delhi, 2012.

Course Outcomes (COs):

1. Employ hardware and software development and debugging tool. (PO – 5, PSO – 2)
2. Write, compile and debug assembly language program. (POs – 1, 2, 3, 5, PSO – 2)
3. Develop C programs for different applications. (POs – 1, 2, 4, 5, PSO – 2)
4. Write C language programs to interface modules to MSP430 microcontroller. (POs –1, 2, 4, 5, PSO – 2, 3)
5. Write assembly language programs to use GPIO ports and timer module of MSP430 microcontroller. (PO – 10, PSO – 2)

DEPARTMENT ELECTIVES

POWER ELECTRONICS

Course Code: ECE01   **Credits: 3:0:0:1**
Prerequisites: Analog Electronic Circuits   **Contact Hours: 42**
Course Coordinator/s: Punya Prabha V and Reshma Verma

UNIT – I

Introduction: Application of power electronics, power semiconductor devices, control characteristics of power devices, types of power electronic circuits, peripheral effects.

Thyristors: Static characteristics, two- transistor model, dynamic characteristics turn on and turn-off

Power MOSFET: Structure, operation, concept of pinch-off, steady state characteristics, switching characteristics, gate drive.

IGBT: Structure of punch-through and non-punch-through IGBT, operation, steady state characteristics, switching characteristics.

UNIT – II

DC Choppers: Principle of step-up and step-down chopper.

Power Supplies: Introduction, Linear Series Voltage Regulator, Linear Shunt Voltage Regulator, Integrated Circuit Voltage Regulators, Switching Regulators, Applications.

UNIT – III

Inverters: Principle of operation, performance parameters, single phase half and full bridge inverter with R and RL load.

Uninterruptible Power Supplies: Introduction, Classification, Performance Evaluation, Applications, Control Techniques, Energy Storage.

UNIT – IV

Automotive Applications of Power Electronics: Introduction, Present Automotive Electrical Power System, System Environment, Functions Enabled by Power Electronics, Multiplexed Load Control, and Electromechanical Power Conversion, Dual/High Voltage Automotive Electrical Systems, Electric and Hybrid Electric Vehicles.

UNIT – V
Non-conventional energy sources: Photovoltaic cells, wind power, LED light circuits.

Self Study: Conduct experiments on Static characteristics of Power MOSFET, IGBT, SCR,RC half-wave and full-wave triggering circuit for a thyristor, SCR firing circuit using synchronized

UJT relaxation circuit, Commutation circuits for thyristor – LC circuit and Impulse commutation circuit, Voltage impulse commutated chopper, Series Inverter.

Textbooks:

1. M. H. Rashid, "Power Electronics: Circuits, Devices and Applications", 3rd Edition, Prentice Hall India, 2011.
2. M. H. Rashid, "Power Electronics Handbook", 3rd Edition, Elsevier Inc., 2011

References:

1. Vedam Subramanyam, "Power Electronics", Revised 2nd Edition, New Age International Publishers, 2008.

Course Outcomes (COs):

1. Describe the structure, characteristics and operation of power semiconductor devices like Thyristor, MOSFET and IGBT. (PO – 1, PSO – 2)
2. Analyze detailed operation of Power supplies. (POs – 1, 2, PSO – 2)
3. Illustrate the various operations of UPS. (POs – 2, 3, PSO – 2)
4. Investigate the various automotive applications of power electronics (POs – 2, 3, PSO – 2)
5. Analyze electronic ballast for discharge lamps. (POs – 3, 5, 9, PSO – 2)

RANDOM VARIABLES AND RANDOM PROCESS

Course Code: ECE02   **Credits: 3:0:0:1**
Prerequisites: Engineering Mathematics   **Contact Hours: 42**
Course Coordinator: Sadashiva V. Chakrasali

UNIT – I

Introduction: Set theory, definitions, conditional probability, Bayes theorem, combined experiments.

Specific Random Variables: Gaussian random variable, other distributions, density functions and examples, conditional distribution and density functions.

UNIT – II

Operations on one random variable: Introduction, Expectation, moments, functions that give moments, Transformations of random variables, computer generation of one random variable.

Multiple random variables: Introduction, vector random variables, joint distribution and its properties, joint density and its properties, conditional distributions and density functions, statistical independence.

UNIT – III

Multiple random variables: Distribution and density function of sum of random variables, central limit theorem.

Random Processes: Introduction, the random process concept, stationarity and independence, correlation functions, measurement of correlation functions.

UNIT – IV

Random Processes: Ergodic processes, Gaussian random processes, Poisson random processes, Wiener Processes.

Spectral Characteristics of Random Processes: Power density spectrum and its properties, white noise.

UNIT – V

Analysis and Processing of Random Processes: Response of linear systems to random inputs, cross power density spectrums, Noise bandwidth, Band pass and band limited processes, modeling of noise processes.

Self Study: Probability: Set definitions, set operations, probability introduced through sets, joint and conditional probability, independent events and Bernoulli trials, Random Variable: the random variable concept, distribution function, density function.

Textbook:

1. Peyton Z. Peebles, "Probability, Random Variables and Random Signal Principles", 4th Edition, McGraw Hill, 2007.
2. A. Papoulis and S. U. Pillai, "Probability, Random Variables and Stochastic Processes", 4th Edition, McGraw Hill, 2012.

References:

1. Hwei P. Hsu, "Theory and Problems of Probability, Random Variables, and Random Processes", Schaum's Outline Series, McGraw Hill, 1997.
2. H Stark and J W Woods, "Probability and Random Processes with applications to Signal Processing", 3rd Edition, Pearson Education, 2002.

Course Outcomes (COs):

1. Solve basic probability and random variable problems. (POs – 1, 2, PSOs – 1, 3)
2. Identify different random variables and their properties. (POs – 1, 2, PSOs – 1, 3)
3. Estimate statistical parameters of different random variables. (POs – 1, 2, PSOs – 1, 3)
4. Classify different random processes. (POs – 1, 2, PSOs – 1, 3)
5. Relate input and output processes of a LTI system. (POs – 1, 2, PSOs – 1, 3)

SPEECH PROCESSING

Course Code: ECE03   **Credits: 3:0:0:1**
Prerequisites: Digital Signal Processing   **Contact Hours: 42**
Course Coordinator: Sadashiva V. Chakrasali

UNIT – I

Digital Models for the Speech Signal: The process of speech production, the acoustic theory of speech production, lossless tube models.

UNIT – II

Time Domain Models for Speech Processing: Time dependent processing of speech, short time energy and average magnitude, speech and silence determination, pitch period estimation.

UNIT – III

Digital Representations of the Speech Waveform: Sampling speech signals, Instantaneous quantization and adaptive quantization, delta modulation, differential PCM.

UNIT – IV

Short Time Fourier analysis and Homomorphic speech processing: Design of digital filter banks, spectrographic displays, pitch detection, analysis by synthesis, analysis – synthesis systems.

Homomorphic speech processing: The complex cepstrum of speech, Pitch detection, formant estimation.

UNIT – V

Linear Predictive Coding: Linear predictive coding of speech: basic principles of linear predictive analysis, computation of the gain for the model, solution of the LPC equations, relations between various speech parameters, synthesis of speech from linear predictive parameters.

Self Study: Digital models for speech signals, short time average zero crossing rates, direct digital code conversion, implementation of filter bank summation method using FFT, applications of LPC parameters.

Textbooks:

1. L R Rabiner and R W Schafer, "Digital Processing of Speech Signals", Pearson Education, 2004.
2. Thomas F. Quatieri, "Discrete Time Speech Signal Processing", Pearson Education, 2009.

References:

1. L. Rabiner, R Schafer, "Theory and Applications of Digital Speech Processing", 1st Edition, Pearson Education, 2010.
2. I. McLoughlin, "Applied Speech and Audio Processing: with Matlab Examples", 1st Edition, Cambridge University Press, 2009.

Course Outcomes (COs):

1. Compare various speech production models. (POs – 2, 3, PSO – 3)
2. Find various speech parameters. (POs – 2, 3, PSO – 3)
3. Represent speech signal in different codes. (POs – 2, 3, 5, PSO – 3)
4. Interpret and analyze speech signals in frequency domain. (POs – 2, 3, PSO – 3)
5. Determine LPC parameters for given speech signal. (POs – 2, 3, 5, PSO – 3)

LOW POWER VLSI DESIGN

Course Code: ECE04   **Credits: 3:0:0:1**
Prerequisites: CMOS VLSI Design   **Contact Hours: 42**
Course Coordinator: V. Anandi

UNIT – I

Power Dissipation in CMOS: Introduction: Need for low power VLSI chips, sources of power consumption, introduction to CMOS inverter power dissipation, low power VLSI design limits, basic principle of low power design.

UNIT – II

Power Optimization: Logical Level Power Optimization: gate reorganization, local restructuring, signal gating, logic encoding, state machine encoding, pre-computation logic

Circuit Level Power Optimization: Transistor and gate sizing, equivalent pin ordering, network restructuring and re-organization, special latches and flip-flops.

UNIT – III

Design of Low Power CMOS Circuits: Reducing power consumption in memories: low power techniques for SRAM, Circuit techniques for reducing power consumption in adders and multipliers.

Special techniques: Power reduction and clock networks, CMOS floating gate, low power bus, delay balancing.

UNIT – IV

Power Estimation: Simulation power analysis: SPICE circuit simulation, Gate level Simulation, Architectural level analysis, Data correlation analysis in DSP systems, Monte-Carlo simulation.

Probabilistic Power analysis: Random signals, probabilistic techniques for signal activity estimation, propagation of static probability in logic circuits, gate level power analysis using transition density.

UNIT – V

Synthesis for Low Power: Behavioral level transforms, algorithm level transforms for low power, architecture driven voltage scaling, power optimization using operation reduction, operation substitution, Bus switching activity.

Self Study: Basic principle of low power design, Signal gating, Network restructuring and re-organization, CMOS floating gates, delay balancing in multipliers, SPICE circuit simulation, Random signals, power optimization using operation reduction

Textbooks:

1. Gary Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic, 1998.
2. K. Roy and S.C. Prasad, "Low Power CMOS VLSI Circuit Design", Wiley, 2000.

References:

1. Jan M. Rabaey and Massoud Pedram, "Low Power Design Methodologies", Kluwer Academic, 2010.
2. P. Chandrakasan and R.W. Broadersen, "Low Power Digital CMOS Design", Kluwer Academic, 1995.
3. NPTEL Lecture series on, "Low power Circuits and Systems", June 2012.

Course Outcomes (COs):

1. Identify the sources of power dissipation in CMOS circuits. (POs –1, 2, 4, 9, PSO – 2)
2. Investigate low power design techniques. (POs – 2, 4, 6, PSO – 2)
3. Apply optimization and trade-off techniques that involve power dissipation of digital circuits. (POs – 2, 5, 6, PSO – 2)
4. Perform power analysis using simulation and probabilistic based approaches. (POs – 4, 9, 11, PSO – 2)
5. Analyze and design low-power VLSI circuits using current generation design style and process technology. (POs – 2, 4, 5, 11, PSO – 2)

OBJECT ORIENTED PROGRAMMING WITH C++

Course Code: ECE05
Prerequisite: Data Structures using C
Course Coordinator: K. Indira

Credits: 3:0:0:1
Contact Hours: 42

UNIT – I

Introduction: Structure of C++ program: Preprocessor directive, declarations and definitions. Functions: Passing simple function, passing arguments to functions such as variables, reference arguments pointer type, function return data type such as constant, variables, data structures, specifying a class, member functions and member data, nested classes, static data members and member functions, friendly functions.

UNIT – II

Classes and Objects: Definition, class initialization, class constructors, destructors, constructor types, multiple constructor in a class, destructors, inheritance, defining derived classes, different types of inheritance, Virtual base classes, abstract classes, constructors in derived classes, virtual functions and dynamic polymorphism, Pure virtual function.

UNIT – III

Operator Overloading: Overloading using various operators, Overloading using friends, Function Overloading, Templates: Function Templates, Class Templates, Header File and Implementation File of a Class Template

UNIT – IV

Pointers: Pointer data types and Pointer Variables, Dynamic Arrays, Classes and Pointers, Overloading the array index operator.

Standard Template Library: Components of STL, Sequence Container, Iterators and Programming Examples

UNIT – V

Stacks: Implementation of Stacks as Arrays, Linked implementation of Stacks, Applications of Stacks.

Queues: Implementation of Queues as Arrays, Linked implementation of Queues
Trees: Basic terminologies of binary trees, Binary Tree Traversal, Binary Search Trees

Self Study: Programs using C++ for the following topics: Introduction to C++ Programming**,** Data types in C++**,** Manipulators and Functions, Structures, Recursive function and Class, Nested Member Functions and Arrays, Static variables, Static Member Function, Arrays of objects and objects as Arguments, Friend Functions and Constructors, Inheritance, Multiple Inheritance and Virtual Functions, Stacks, Queues, Trees and Hashing.

Textbooks:

1. E. Balaguruswamy**, "**Object Oriented Programming with C++", 4th Edition, TMH, 2011.
2. D. S. Malik, "Data Structures using C++", Indian Edition, Cengage Learning, 2003.

References:

1. Robert Lafore, "Introduction to OOPs with C++", 4th Edition, Sams Publishing, 2001.
2. Sartaj Sahni, "Data Structures, Algorithms and Applications in C++", International Edition, McGraw Hill, 2000.
3. Gray Litwin, "Programming with C++ and Data Structures", Vikas Publications, 2003.

Course Outcomes (COs):

1. Illustrate the concept of C++ program by using functions with different arguments. (POs – 1, 2, 3, 5, 12, PSO – 2)
2. Apply the concept of inheritance in solving real world problems. (POs – 2, 3, 5, 12,PSO – 2)
3. Employ overloading concepts to overload built in operators. (POs – 2, 3, 5, 12, PSO – 2)
4. Use pointers for dynamic arrays and linked lists. (POs – 2, 3, 5, 12, PSO – 2)
5. Implement the concept of stack, queues and trees using Standard Template Library. (POs – 2, 3, 5, 12, PSO – 2)

DIGITAL SYSTEM DESIGN USING VERILOG

Course Code: ECE06   **Credits: 3:0:0:1**

Prerequisite: Digital Electronics   **Contact Hours: 42**

Course Coordinator: Lakshmi Shrinivasan

UNIT – I

Introduction and Methodology: Digital systems and embedded systems, Real world circuits, Models, Design Methodology.

Combinational Basics: Boolean function and Boolean Algebra, Binary coding, Combinational components and circuits.

UNIT – II

Sequential Basics: Counters, Sequential data paths and controls, Clocked synchronous timing methodology, Memories: Concepts, Memory types, Error detection and correction.

UNIT – III

Implementation Fabrics: ICs, PLDs, Interconnections and signal integrity, Processor Basics: Embedded computer organization, Instruction and data.

UNIT – IV

Interfacing with memory and I/O Interfacing: I/O devices, I/O Controllers, Parallel Buses, Serial transmission, I/O software.

UNIT – V

Accelerators: General concepts, **Case study:** Video edge detection, verifying an accelerator.

Design Methodology: Design optimization, Design for test.

Self Study: Binary representation and circuit elements, Sequential Basics: Storage elements, Packaging and circuit boards, Design methodology: Design Flow.

Textbook:

1. Peter J. Ashenden, "Digital design: An Embedded systems approach using Verilog", Morgan Kaufmann Publishers, Elsevier, 2014.

References:

1. Samir Palnitkar, "Verilog HDL: A guide to digital design and synthesis", 2nd Edition, Pearson Publications, 2009.
2. Stephen Brown, ZvonkoVranesic, "Fundamentals of Digital Logic with Verilog Design", 2nd Edition, Tata McGraw Hill Publications. 2009.

Course Outcomes (COs):

1. Describe the basics of combinational components for building digital systems. (POs – 1, 3, PSOs – 1, 2)
2. Apply the sequential basics and memory concepts to build a specified digital system (POs – 1, 2, 3, PSOs – 1, 2)
3. Implement processors and other digital systems on programmable logic devices. (POs – 1, 2, 3, 4, PSOs – 1, 2)
4. Interface different I/O and memory modules in a system. (POs – 1, 2, 3, PSOs – 1, 2)
5. Illustrate the entire digital system design flow. (POs – 1, 2, 3, PSOs – 1, 2)

DSP ARCHITECTURE AND ALGORITHMS

Course Code: ECE07   **Credits: 3:0:0:1**
Prerequisites: Digital Signal Processing   **Contact Hours: 42**
Course Coordinator: Maya V. Karki

UNIT – I

Introduction to Digital Signal Processors: A Digital Signal Processing System, Programmable digital signal processors, major features of programmable digital signal processors, architectures for programmable digital signal processing devices, introduction to basic architectural features.

Architecture and Instruction Set of C6x processor: TMS320C6x architecture, functional units, fetch and execute units, pipelining, registers, linear and circular addressing modes, instruction sets.

UNIT – II

Software and Memory Consideration of C6x processor: Assembler directives, Linear assembly, ASM statements within C, C callable assembly function, timers, interrupts, multichannel buffered serial ports, direct memory access, memory considerations, fixed and floating point format, code improvements, constraints, Programming examples using assembly and linear assembly.

UNIT – III

Implementation of FIR filters: FIR filters, FIR lattice structure, FIR implementation using Fourier series, window functions, Programming example using ASM and C.

UNIT – IV

Implementation of IIR filters: Introduction, IIR filter structures, Bilinear transformation, Programming examples based on ASM and C.

UNIT – V

Fast Fourier Transform: Introduction, development of FFT algorithm with Radix-2, Decimation in frequency FFT algorithm with Radix-2, Decimation in Time FFT algorithm with Radix-2, Bit reversal for unscrambling, development of FFT algorithm with Radix-4, Inverse fast Fourier transform.

Self Study: Assembly code format, Programming examples using assembly and linear assembly, Programming example using ASM on FIR and IIR filtering, Programming example using ASM on FFT.

Textbook:

1. Rulph Chassaing, Donald Relay, "Digital Signal Processing and Applications with TMS3206713 and TMS320C6416DSK", 2nd Edition, Wiley 2014.

References

1. Sen M. Kuo, Woon-Seng S. Gan, "Digital Signal Processors: Architectures, Implementations and Applications", Pearson Prentice Hall, 2005
2. Lapsley, "DSP Processor Fundamentals, Architectures & Features", S. Chand & Co, 2000.

Course Outcomes (COs):

1. Distinguish the computational building blocks, architectural features and instruction sets of TMS320C6x. (POs–1, 2, 3, PSO–3)
2. Compute the programming examples using assembly and linear assembly. (POs – 2, 3, 5, PSO – 3)
3. Demonstrate the implementation of FIR filters using ASM and C. (POs – 2, 3, 5, PSO – 3)
4. Employ ASM and C code to realize IIR filtering. (POs – 2, 3, 5, PSO – 3)
5. Illustrate realization of FFT algorithm with Radix-2 and Radix-4. (POs – 2, 3, 5, PSO – 3)

MICRO ELECTRO MECHANICAL SYSTEMS

Course Code: ECE08   **Credits: 3:0:0:1**
Prerequisites: CMOS VLSI Design   **Contact Hours: 42**
Course Coordinator: Lakshmi S

UNIT – I

Introduction to MEMS: Historical background of Micro Electro Mechanical Systems, multi-disciplinary aspects, basic technologies, application areas, scaling laws in miniaturization, scaling in geometry, electrostatics, electromagnetics, electricity and heat transfer.

UNIT – II

Micro Systems – Principles: Transduction principles in MEMS Sensors: Various sensing mechanisms, Actuators: different actuation mechanisms - silicon capacitive accelerometer, piezo-resistive pressure sensor, blood analyzer, conductometric gas sensor, silicon micro-mirror arrays, piezo-electric based inkjet print head, electrostatic comb-drives.

UNIT – III

Materials and Micromanufacturing: Semiconducting materials, Silicon, Silicon dioxide, Silicon Nitride, Quartz, Poly silicon, Polymers, Materials for wafer processing, Packaging materials, Silicon wafer processing, lithography, thin-film deposition, etching (wet and dry), wafer-bonding, Silicon micromachining: surface, bulk, LIGA process.

UNIT – IV

Electrical and Electronics Aspects: Electrostatics, Coupled electro mechanics, stability and Pull-in phenomenon, Practical signal conditioning circuits for micro systems, RF MEMS: Switches, varactors.

UNIT – V

Integration and Packaging of Micro electromechanical Systems: Integration of microelectronics and micro devices at wafer and chip levels, Microelectronic packaging: wire and ball bonding, flip chip, Micro system packaging examples.

Self Study: Feynman's vision, Smart phone applications, Smart buildings, Wafer bonding process, Tuned filters, Application circuits based on microcontrollers for pressure sensor, Accelerometer, Testing of Micro sensors, Qualification of MEMS devices.

Textbooks:

1. G. K. Ananthasuresh, K. J. Vinoy, S. Gopalakrishnan, K. N. Bhat, V. K. Aatre, "Micro and Smart Systems", 1st Edition, Wiley India, 2010.
2. T R Hsu, "MEMS and Microsystems Design and Manufacturing", 2nd Edition, Tata McGraw Hill, 2008 .

References:

1. Chang Liu, "Foundations of MEMS", Pearson International Edition, 2006.
2. S D Senturia, "Microsystem Design", Springer International Edition, 2001.

Course Outcomes (COs):

1. Recognize the multidisciplinary and scaling aspects of micro systems. (POs – 1, 2, 3, 4, PSOs – 2, 3)
2. Analyze the various transduction mechanisms and applications of MEMS. (POs – 1, 2, 3, 4, PSOs – 2, 3)
3. Describe the various fabrication processes of MEMS devices. (POs – 2, 9, 10, 12, PSOs – 2, 3)
4. Analyze the electronics aspects of MEMS systems. (POs – 1, 2, 3, 4, PSOs – 2, 3)
5. Classify the various packaging methods for MEMS devices. (POs – 2, 3, 4, PSOs – 2, 3)

ARTIFICIAL NEURAL NETWORKS AND FUZZY LOGIC

Course Code: ECE09   **Credit: 3:0:0:1**
Prerequisites: Digital Signal Processing   **Contact Hours: 42**
Course Coordinator/s: Punya Prabha V

UNIT – I

Fundamentals of Neural Networks: Biological neurons and their artificial models, Neural Network Architecture: Single Layer, Multi-layer Feed Forward Networks, Recurrent Networks, Learning methods, Applications.

UNIT – II

Back Propagation Networks: Architecture of a back propagation network, Back propagation learning, Training of Neural network, Method of steepest descent, effect of learning rate, Back propagation algorithm, Radial Basis Function Network (RBFN), Applications.

UNIT – III

Adaptive Resonance Theory (ART): Introduction, Cluster Structure, Vector Quantization, Classical ART Networks, Simplified ART Architecture, Special features of ART1 models, ART1 Algorithms, Illustration, Applications.

UNIT – IV

Fuzzy Set Theory: Fuzzy vs crisp sets, crisp sets, Operations on crisp sets, Properties of crisp sets, Partition and Covering, Membership function, Basic fuzzy set operations, Properties of Fuzzy sets, Crisp relations and Fuzzy relations, Applications.

UNIT – V

Fuzzy systems: Crisp logic: Laws of propositional logic, inference in propositional logic, Predicate logic: Interpretations of predicate logic formula, inference in predicate logic, Fuzzy logic: Fuzzy Quantifiers, Fuzzy inference, Fuzzy rule based system, defuzzification.

Applications: Greg Viot's Fuzzy cruise controller, Air conditioner controller.

Self Study: Implementation: Pattern classification using Hebb net and McCulloch–Pitts net, Pattern recognition using Perceptron Networks, Implementation of all fuzzy operations on both discrete and continuous fuzzy sets, Defuzzification, Fuzzy inference system.

Textbooks:

1. Rajasekaran. S, Vijayalakshmi Pai G.A, "Neural networks, Fuzzy logic, and Genetic Algorithms, Synthesis and Applications", PHI New Delhi, 2011.
2. S. N. Sivanandam, S. Sumathi, S N Deepa , "Introduction to Neural Networks using Matlab 6.0", Tata McGraw Hill, 2006.

References:

1. Simon Haykin, "Neural Networks: A Comprehensive Foundation", 3rd Edition, PHI, 2009.
2. Timothy J Ross, "Fuzzy Logic with Engineering Applications", 3rd Edition, Wiley, India, New Delhi, 2011.

Course Outcomes (COs):

1. Describe the relation between real brains and simple artificial neural network models. (POs – 1, 6, 12, PSO – 2)

2. Select different neural network algorithms for suitable applications. (POs – 1, 3, 6, 12, PSO – 2)

3. Identify the main implementation issues for common neural network systems and apply ANN models to data compression and pattern identification. (POs – 1, 3, 6, 12, PSO – 2)

4. Apply the rules of fuzzy logic for fuzzy controller. (POs – 2, 4, 6, 12, PSO – 2)

5. Employ fuzzy set operations and defuzzification for a given application. (POs – 1, 2, 4, 6, 12, PSO – 2)

IMAGE PROCESSING

Course Code: ECE10   **Credit: 3:0:0:1**
Prerequisites: Digital Signal Processing   **Contact Hours: 42**
Course Coordinator: Shreedarshan K

UNIT – I

Introduction and Fundamentals: What is Digital Image Processing? Origins, Examples, fundamental steps in Digital Image Processing, Components of an image processing system, Elements of visual perception, Image sensing and acquisition, Image sampling and quantization, some basic relationships between pixels, mathematical tools used in image processing.

UNIT – II

Intensity Transformations and Spatial Filtering: Basic intensity transformation functions, Histogram processing, spatial filtering, smoothing spatial filters, sharpening spatial filters.

UNIT – III

Image Transforms: Two dimensional orthogonal and unitary transforms, property of unitary transforms, 1D-DFT, 2D-DFT, DCT, Basics of filtering in the frequency domain, image smoothing and image sharpening using frequency domain filters.

UNIT – IV

Image Segmentation – 1: Fundamentals, Detection of discontinuities, line detection, Edge detection, Edge linking via Hough Transform, Thresholding, Basics of intensity thresholding, Basic global thresholding, Optimum global thresholding using Otsu's method.

UNIT – V

Image Segmentation and Morphological Image Processing: Region based segmentation: Region growing, splitting and merging, Dilation and Erosion, some basic morphological algorithms, segmentation using morphological watersheds.

Self Study: Implement programs for image processing basics, reading and display of image, histogram, image sensing, acquisition and sampling, intensity transformations and filtering, DFT, DCT, thresholding of images, image segmentation and morphological algorithms.

Textbooks:

1. R. C. Gonzalez, R. E. Woods, "Digital Image Processing", 3rd Edition, Pearson Education, 2009.
2. R. C. Gonzalez, R. E. Woods, S. L. Eddins, "Digital Image Processing using Matlab", 2nd Edition, Mc Graw hill, 2010.

References:

1. Anil K. Jain, "Fundamentals of Digital Image Processing", Pearson Education, 2002.

Course Outcomes (COs):

1. Analyze general terminology of digital image processing. (POs – 1, 2, 3, 5, PSO – 3)
2. Examine various types of images, intensity transformations and spatial filtering. (POs – 2, 3, 5, PSO – 3)
3. Employ Fourier Transform for image processing in frequency domain. (POs – 1, 2, 3, 5, PSO – 3)
4. Apply segmentation algorithms to detect and link edges in an image. (POs – 3, 5, PSO – 3)
5. Develop morphological algorithms to describe the shape of a region in an image. (POs – 2, 3, 5, PSO – 3)

REAL TIME SYSTEMS

Course Code: ECE11
Prerequisite: Microprocessors
Course Coordinator: Lakshmi Shrinivasan

Credits: 3:0:0:1
Contact Hours: 42

UNIT – I

Fundamentals of Real Time Systems: Concepts and Misconceptions, Multi-disciplinary Design Challenges, Birth and Evolution of Real-Time Systems.

Hardware for Real Time Systems: Basic Processor Architecture, Memory Technologies, Architectural Advancements, Peripheral Interfacing, Microprocessor versus Microcontroller, Distributed Real-Time Architectures.

UNIT – II

Real Time Operating systems: From Pseudo kernels to Operating Systems, Theoretical Foundations of Scheduling, System Services for Application Programs, Memory Management Issues, and Selecting Real-Time Operating Systems.

UNIT – III

Programming Languages for Real-Time Systems: Coding of Real-Time Software, Assembly Language, Procedural Languages, and Object-Oriented Languages, Overview of Programming Languages, Automatic Code Generation, and Compiler Optimizations of Code.

UNIT – IV

Requirements Engineering Methodologies: Requirements Engineering for Real-Time Systems, Formal Methods in System Specification, Semiformal Methods in System Specification, The Requirements Document.

UNIT – V

Software Design Approaches: Qualities of Real-Time Software, Software Engineering Principles, Procedural Design Approach, Object-Oriented Design Approach, Life Cycle Models.

Self Study: Advancements behind Modern Real-Time Systems, Hierarchical Memory Organization, Time-Triggered Architectures, and Memory Management in the Task Control Block Model, Case Study: Selecting a Commercial Real-Time Operating System, Cardelli's Metrics and Object-Oriented Languages, Recommendations on Specification Approach, Agile Methodologies.

Textbook:

1. Phillip. A. Laplante, "Real-time systems design and analysis", 2nd Edition, PHI, 2012.

References:
1. Stuart Bennet, "Real-Time Computer Control – An Introduction", 2nd Edition, Pearson Education, 2005.
2. Rob Williams, "Real-Time Systems Development", Elsevier, 2006.
3. Raj Kamal, "Embedded Systems", Tata McGraw Hill, India, 2005.

Course Outcomes (COs):

1. Describe the basics of real time systems. (POs – 1, 2, PSO – 2)

2. Select appropriate scheduling strategy based on real time application constraints. (POs – 3, 4, PSOs – 2, 3)

3. Elaborate the language syntax for real time applications. (POs – 2, 3, PSO – 2)

4. Identify suitable RTS development methodology for a given application. (POs – 3, 4, PSOs – 2, 3)

5. Apply the knowledge of software design specification to build RTS. (POs – 1, 2, 3, 4, PSO – 2)

ADVANCED DIGITAL LOGIC DESIGN

Course Code: ECE12   **Credits: 3:0:0:1**
Prerequisites: Digital Electronic Circuits   **Contact Hours: 42**
Course Coordinator: A. R. Priyarenjini

UNIT – I

Digital Integrated Circuits: Technology Scaling, Die size growth, Frequency, Power dissipation, Challenges in digital design, Design metrics, Cost of Integrated circuits, ASIC, Evolution of SoC, ASIC flow vs SoC flow, SoC design challenges.

Introduction to CMOS Technology: CMOS operation principles, Characteristic curves of CMOS, CMOS inverter and characteristic curves, Delays in inverters, Buffer Design, Power dissipation in CMOS, CMOS Logic, Stick diagrams and Layout diagrams, Timing concepts.

UNIT – II

Digital Building Blocks: Decoder, encoder, code converters, Priority encoder, multiplexer, Demultiplexer, Comparators, Parity check schemes, Multiplexer, De-multiplexer, Pass Transistor Logic, Application of multiplexer as a multi-purpose logical element, asynchronous and synchronous up-down counters, Shift registers.

FSM Design: Mealy and Moore modeling, Adder & Multiplier concepts.

UNIT – III

Logic Design using Verilog: Lexical Conventions, Data Types, Modules, Nets, Values, Data Types, Comments, arrays in Verilog, Expressions, Operators, Operands, Arrays, memories, Strings, Delays, parameterized designs, Procedural blocks, Blocking and Non-Blocking assignment, looping, flow Control, Task, Function, Synchronization, Event Simulation, need for verification, basic test bench generation and simulation.

UNIT – IV

Principles of RTL Design: Verilog coding concepts, Verilog coding guide lines: Combinational, Sequential, FSM, general guidelines, synthesizable Verilog constructs, sensitivity list, Verilog events, RTL design challenges, clock domain crossing, Verilog modeling of combinational logic, Verilog modeling of sequential logic.

UNIT – V

Design and simulation of architectural building blocks: Basic Building blocks, design using Verilog HDL: Arithmetic Components – Multiplier design, Data Integrity – Parity Generation circuits, Control logic – Arbitration, FSM Design, overlapping and non-overlapping Mealy and Moore state machine design

Mini-Project: n bit simple ALU design & verification

Self Study: Moore's law, PMOS& NMOS operation, basic gates, universal gates, NAND & NOR CMOS implementation, Evolution & importance of HDL, Introduction to Verilog, Levels of abstraction, typical design flow, design using Verilog HDL, Arithmetic components
– Adder, Subtractor.

Textbooks:

1. Morris Mano M, "Digital Design", 4th Edition, Pearson Education, 2014.
2. Neil H. E. Weste, David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 3rd Edition, Pearson Education, 2004.
3. Samir Palnitkar, "VERILOG HDL – A guide to digital design and synthesis", 2nd Edition, Pearson Education, 2003.

References:

1. J. Bhasker, "Verilog HDL Synthesis: A Practical Primer", 3rd Edition, Star Galaxy, 2005.
2. A. Anand Kumar, "Fundamentals of Digital Circuits", 2nd Edition, PHI Learning, 2012.

Course Outcomes (COs):

1. Understand the basic VLSI design principles. (POs – 1, 2, 3, 4, PSO – 2)
2. Apply basic digital design principles to complex circuits. (POs – 1, 2, 3, 4, 5, PSO – 1, 2)
3. Employ Verilog HDL for describing digital circuits. (POs – 1, 2, 3, 4, 5, PSO – 2)
4. Create directed test benches, run simulators and analyze/debug. (POs – 1, 2, 3, 4, 5, PSO – 2).
5. Employ FSMs for the design of basic sub circuits and use EDA tools to simulate them. (POs – 1, 2, 3, 4, 5, PSO – 2).

ADVANCED DIGITAL LOGIC VERIFICATION

Course Code: ECE13   Credits: 3:0:0:1
Prerequisites: Advanced Digital Logic Design   Contact Hours: 42
Course Coordinator: S. L. Gangadharaiah

UNIT – I

Verification Concepts: Concepts of verification, Test bench generation, Functional verification approaches, Typical verification flow, Stimulus generation, Direct testing.

Coverage: Code coverage and Functional coverage, Coverage plan.

UNIT – II

System Verilog – language constructs: System Verilog constructs–Data types, two state data, strings, Arrays: Queues, Dynamic and Associative Arrays, Structs, Enumerated types. Program blocks, modules, interfaces, Clocking ports, Mod ports.

UNIT – III

System Verilog – Classes: Classes and Objects, Class Variables and Methods, Class Instantiation, Inheritance and Encapsulation, Polymorphism.

Randomization: Directed vs Random Testing, Randomization: Constraint driven Randomization.

UNIT – IV

System Verilog – Assertions and Coverage: Introduction to assertion based verification, Immediate and concurrent assertions

Coverage driven assertion: Motivation, types of coverage, Cover group, Cover point, Cross coverage, Concepts of binning and event sampling.

UNIT – V

Building Test bench: Layered test bench architecture, Introduction to universal verification methodology, Overview of UVM.

Self Study: Importance of verification, Stimulus vs verification, Language evolution, Introduction to universal verification methodology, Base classes and simulation phases in UVM and UVM macros, Unified messaging in UVM, UVM environment structure, Connecting DUT – Virtual Interface.

Tools: NCVerilog, NCSim, VCSMX for System Verilog.

References:

1. System Verilog LRM
2. Chris Spear, Greogory J Tumbush, "System Verilog for Verification – A guide to learning test bench language features", Springer, 2012.
3. Sasan Iman, "Step by Step functional Verification with System Verilog and OVM", Hansen Brown Publishing, 2008

Reference Websites: www.testbench.in,www.asic-world.com

Online material: Seer recordings

Course Outcomes (COs):

1. Express the principle of HDL verification. (POs – 2, 3, 4, 5, PSO – 2)
2. Apply OOPs concepts in System Verilog. (POs – 2, 3, 4, 5, PSO – 2)
3. Build basic verification environment using System Verilog. (POs – 2, 3, 4, 5, PSO – 2)
4. Generate random stimulus and track functional coverage using System Verilog. (POs – 2, 3, 4, 5, PSO – 2)
5. Appreciate the concepts of layered test bench architecture and its components. (POs – 2, 3, 4, 5, PSO – 2)

LINEAR ALGEBRA

Course Code: ECE14   **Credits: 3:0:0:1**
Prerequisite: Engineering Mathematics   **Contact Hours: 42**
Course Coordinator: Shreedarshan K

UNIT – I

Linear Equations: Systems of Linear Equations, Row reduction and Echelon Forms, Vector Equations, Matrix Equation Ax = b, Solution Sets of Linear Systems, Linear Independence, Introduction to Linear Transformations, Matrix of a Linear Transformation, Applications.

UNIT – II

Vector Spaces: Vector Spaces and Subspaces, Null Spaces, Column Spaces and Linear Transformations, Linearly Independent sets, Bases, Co-ordinate Systems, The Dimension of a Vector Space, Rank.

UNIT – III

Eigen Values and Eigen Vectors: The Characteristic equation, Diagonalization, EigenVectors and Linear Transformations.

UNIT – IV

Orthogonality and Least Squares: Orthogonal Sets, Orthogonal Projections, Gram–Schmidt Process, Least Squares Problems.

UNIT – V

Symmetric Matrices and Quadratic Forms: Diagonalization of Symmetric Matrices, Quadratic Forms, Singular Value Decomposition.

Self Study: Linear models in engineering, Applications to difference equations, Inner Product, Length and Orthogonality, Constrained Optimization.

Textbooks:

1. David C Lay, Stephen R Lay, Judi J McDonald, "Linear Algebra and its Applications", 5th Edition, Pearson Education, 2015.
2. Gilbert Strang, "Linear Algebra and its Applications", 4th Edition, Thomson Learning Asia, 2007.

References:

1. S Lipschutz, M Lipson, "Schaum's Outline of Linear Algebra", 5th Edition Mc Graw hills, 2012.
2. M J Sterling, "Linear Algebra for Dummies", 1st Edition, John Wiley & Sons Ltd, 2009.

Course Outcomes (COs):

1. Solve systems of linear equations using multiple methods, including Gaussian elimination, matrix inversion and matrix operations. (POs – 1, 2, 3, PSO – 3)
2. Demonstrate understanding of the concepts of vector space and subspace. (POs – 2, 3, 5, PSO – 3)
3. Demonstrate understanding of linear independence, span and basis. (POs – 2, 3, 5, PSO – 3)
4. Determine eigen values and eigenvectors and solve eigen value problems. (POs – 2, 3, 5, PSO – 3)
5. Apply principles of matrix algebra to linear transformations. (POs – 2, 3, 5, PSO – 3)

MACHINE LEARNING

Course Code: ECE15   **Credits: 3:0:0:1**
Prerequisite: Linear Algebra   **Contact Hours: 42**
ourse Coordinator: S. Sethu Selvi

UNIT – I

Introduction: Probability theory, what is machine learning, example machine learning applications.

Supervised Learning: Learning a class from examples, VC dimension, PAC learning, Noise, Learning multiple classes, Regression, Model selection and generalization.

UNIT – II

Bayesian Learning: Classification, losses and risks, utility theory MLE, Evaluating an estimator, Bayes estimator, parametric classification.

Discriminant functions: Introduction, Discriminant functions, Least squares classification, Fisher's linear discriminant, fixed basis functions, logistic regression.

UNIT – III

Multivariate methods: Multivariate data, Parameter Estimation, Estimation of Missing Values, Multivariate Normal Distribution, Multivariate Classification, Tuning Complexity, Discrete Features, Multivariate Regression.

Non-parametric methods: Nearest Neighbor Classifier, Nonparametric Density Estimation.

UNIT – IV

Maximum margin classifiers: SVM, Introduction to kernel methods, Overlapping class distributions, Relation to logistic regression, Multiclass SVMs, SVMs for regression.

Mixture models and EM: K–means clustering, Mixture of Gaussians, Hierarchical Clustering, Choosing the Number of Clusters.

UNIT – V

Dimensionality reduction: Combining Models.

Self Study: Implementation of Histograms, Covariance matrices, Regression with sampling, Bayes classifier, Perceptron algorithm and clustering algorithms.

Textbooks:

1. Ethem Alpaydin, "Introduction to Machine Learning", 2nd Edition, PHI Learning Pvt. Ltd, 2010.
2. Christopher Bishop, "Pattern Recognition and Machine Learning", CBS Publishers & Distributors, 2010.

Course Outcomes (COs):

1. Appreciate the concepts and issues of various learning systems. (POs – 1, 2, 3, 4, PSOs – 1, 3)
2. Employ Bayesian learning and discriminant functions for classification. (POs – 1, 2, 3, 4, PSOs – 1, 3)
3. Evaluate multi-variate and non-parametric methods for regression and classification. (POs – 1, 2, 3, 4, PSOs – 1, 3)
4. Describe maximum margin classifiers and mixture models. (POs – 1, 2, 3, 4, PSOs – 1, 3)
5. Examine various dimensionality reduction algorithms. (POs – 1, 2, 3, 4, PSOs – 1, 3)

ANALOG AND MIXED SIGNAL VLSI DESIGN

Course Code: ECE16
Prerequisite: CMOS VLSI Design
Course Coordinator: M. Nagabhushan

Course Credits: 3:0:0:1
Contact Hours: 42

UNIT – I

Single Stage Amplifiers: Common Source stage with different loads and source degeneration, Source follower, Common Gate stage, Cascode structures and Folded Cascode structures.

UNIT – II

Differential Amplifier and Current Mirrors: Introduction to Differential Pair Amplifier, Quantitative Analysis to Differential Pair Amplifier, Common Mode Response, Differential Amplifiers with Different Loads, Effects of mismatches, Simple Current Mirrors, Cascode Current Mirrors, Differential Pair with Current Mirror Load.

UNIT – III

Operational Amplifiers and Frequency Response: Op Amps Low Frequency Analysis, Telescopic Op Amps, Folded Cascode Op Amps, Two Stage Op Amps, Common Mode Feedback. Frequency response of common source amplifiers, Source Follower Common Gate, Cascode Structures and Folded Cascode Structures, Differential Amplifiers, Single Ended Differential Pair.

UNIT – IV

Frequency Compensation and Stability: Frequency compensation techniques in Telescopic Op Amps, Folded Cascode Op Amps, Two Stage Op Amps.

UNIT – V

Data Converters: Analog vs Digital and Discrete time signals, converting analog signals to digital signals, Sample and Hold characteristics, DAC Specifications, ADC Specifications, DAC Architectures, Digital input code, Resistor String, R – 2R Ladder Networks, Current steering, Charge scaling DACs, Cyclic DAC, Pipeline DAC, ADC Architectures. Flash type, 2-Step Flash, Pipeline ADC, Integrating ADC, Successive Approximation methods.

Self Study: Differential amplifiers with different loads, Op-amp low frequency analysis, frequency response of cascode structures, ADC & DAC specifications, cyclic DAC.

Textbooks:

1. B Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGraw Hill Education, 2016.
2. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", Wiley IEEE Press, 3rd Edition, 2010.

References:

1. Tony Chan Carusone, David Johns, Kenneth Martin, "Analog Integrated Circuit Design", 2nd Edition, Wiley, 2011.
2. P E Allen, D R Holberg, "CMOS Analog Circuit Design", 2nd Edition, Oxford University Press, 2002.
3. Gray Paul R, Meyer Robert G, "Analysis and Design of Analog Integrated Circuits", 5th Edition, John Wiley, 2010.
4. Franco Sergio, "Design with Operational Amplifiers and Analog Integrated Circuits", 4th Edition, McGraw Hill, 2011.

Course Outcomes (COs):

1. Appreciate the basic concepts of single amplifier design and cascode Amplifier. (POs – 1, 2, 3, 4, 6, 10, 11, PSOs – 1, 2)
2. Design a multistage amplifier using single stage amplifier concept. (POs – 2, 3, 4, 6, 10, 11, PSOs – 1, 2)
3. Determine the poles and zeroes of a multi-pole system and analyze the frequency response and stability of the system. (POs – 2, 3, 4, 6, 11, PSOs – 1, 2)
4. Design an operational amplifier to optimize its performance metrics. (POs – 1, 2, 3, 4, 6, 8, 10, 11, PSO – 1, 2)
5. Analyze different ADC/DAC architectures. (POs – 1, 2, 3, 4, 6, 8, 10, 11, PSOs – 1, 2)

NEURAL NETWORKS AND DEEP LEARNING

Course Code: ECE17   **Credits: 3:0:0:1**
Prerequisites: Machine Learning   **Contact Hours: 42**
Course Coordinator: S. Sethu Selvi

UNIT – I

Introduction: Human brain, neuron models, neural nets as directed graphs, feedback, neural architectures, knowledge representation, connection to artificial intelligence.

UNIT – II

Learning process: Error-correction learning, memory based learning, Hebbian learning, competitive learning, Boltzman learning, credit assignment, learning with and without a teacher, learning tasks, memory, statistical learning theory.

UNIT – III

Modern practical deep neural networks: Deep feed forward networks, regularization for deep learning, optimization for training deep models, convolutional networks.

UNIT – IV

Sequence Modeling: Recurrent and Recursive nets, Practical Methodology, applications.

UNIT – V

Deep Learning Research: Linear factor models, auto encoders, variational auto encoders, restricted Boltzman machine, generative adversarial networks.

Self Study: Implementation of neural network and deep learning algorithms.

Textbooks:

1. Simon Haykin, "Neural networks: A comprehensive foundation", 2nd Edition, Prentice Hall, New Delhi, 1999.
2. Ian Good fellow, Yoshua Bengio and Aaron Courville, "Deep Learning", MIT Press, 2016.

Course Outcomes (COs):

1. Appreciate the concepts and applications of neural networks and deep learning. (POs – 2, 3, 4, 5, PSOs – 1, 3)

2. Examine how various types of learning work and how they can be used. (POs – 2, 3, 4, 5, PSOs – 1, 3)

3. Apply deep feed forward and convolutional networks to solve practical problems. (POs – 2, 3, 4, 5, PSOs – 1, 3)

4. Demonstrate how recurrent and recursive nets function and how practical problems can be mapped to them. (POs – 2, 3, 4, 5, PSOs – 1, 3)

5. Design end-to-end deep learning architectures involving auto encoders, RBM, and generative adversarial networks for practical applications. (POs – 2, 3, 4, 5, PSOs – 1, 3)